IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	SATOH
Application No.	:	09/830,376
Filed	:	04/25/2001
For	:	A DATA WRITING/READING METHOD, A DE-INTER-LEAVING METHOD, A DATA PROCESSING METHOD, A MEMORY AND A MEMORY DRIVE APPARATUS

APPEAL BRIEF

On Appeal from Group Art Unit 2188

Date: 07/16/2007

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Michael Ure
(Name)

M Ure 11/08/07
(Signature and Date)

I. REAL PARTY IN INTEREST

The real party in interest is NXP B.V., the successor in interest to the present assignee of record of the present application, Koninklijke Philips Electronics N.V., and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1, 3, 4, 6, 7, 9 and 10-18 are pending, all of which stand finally rejected and form the subject matter of the present appeal. Claims 2, 5 and 8 have been canceled.

IV. STATUS OF AMENDMENTS

At the request of the Examiner, an Amendment-After-Final has been submitted correcting the dependency of claim 18.

V. SUMMARY of the CLAIMED SUBJECT MATTER

The present invention relates to the transfer of data to and from memory, particularly for purposes of de-interleaving. In a conventional data de-interleaver, data is written in one direction (row or column) and read in a an opposite direction (row or

IX. APPENDIX: THE CLAIMS ON APPEAL

1. A data writing/reading method of sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that a first plurality of data is written into the memory in a first write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction; wherein when plural data having written into the memory at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.

3. A data writing/reading method as claimed in claim 1, wherein plural data are arranged into the memory in matrix structures having n by n blocks, each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks.

4. A method of de-interleaving by sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that a first plurality of data is written into the memory in a first write direction, the first plurality of data being read from the memory in

a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction; wherein when plural data having written into the memory at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.

6. A de-interleaving method as claimed in claim 4, wherein plural data are arranged into the memory in matrix structures having n by n blocks, each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks.

7. A data processing method comprising a first step of interleaving a plurality of data, and a second step of de-interleaving by sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that a first plurality of data is written into the memory in a first write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction; wherein when plural data having written into the memory at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, on the other hand, when plural data having

written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.

9. A data processing method as claimed in claim 7, wherein the first step contains configuring a super frame having plural frames, each of the frames formed by arranging plural data in matrix form, and contains interleaving the plural data configuring the super frame.

10. A data processing method as claimed in claim 7, wherein the second step is characterize in that interleaved plural data are arranged into the memory in matrix structures having n by n blocks, each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks.

11. A data processing method as claimed in claim 10, wherein the first step is characterized by configuring a super frame having eight frames, each of the frames formed by arranging (203x48) data in matrix form, and is characterized by interleaving (203x48x8) data configuring the super frame, and the second step is characterized in that when (203x48x8) data having written into the memory at present are read in a row direction, (203x48x8) data which is the next to be written are sequentially written in the row direction, on the other hahnd, when (203x48x8) data having written into the memory at present are read in a column direction, (203x48x8) data which is the next to be written are sequentially written in the column direction.

12. A data processing method as claimed in claim 11, wherein the second step is for arranging (203x48x8) data into the memory in 48 matrix structures, each of the 48 matrix structures formed from (203x8) data, and each of the 48 matrix structures is the structure having n by n blocks, each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks.

13. A data processing method as claimed in claim 12, wherein each of the 48 matrix structures is the structure having 8 by 8 blocks, each of the blocks having 26 addresses, and each of the blocks for writing one data into an area corresponding to the one address of each of the blocks, and the second step is for writing one data into the area corresponding to the one address of each of the blocks.

14. A data processing method as claimed in claim 12, wherein each of the 48 matrix structures is the structure having 8 by 8 blocks, each of the blocks having 4 addresses, and each of the blocks for writing 7 data into an area corresponding to the one address of each of the blocks, and the second step is for writing 7 data into the area corresponding to the one address of each of the blocks.

15. A memory for sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that a first plurality of data is written into the memory in a first

write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction; wherein when plural data having written into the memory at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.

16. A memory drive apparatus for sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that a first plurality of data is written into the memory in a first write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction; wherein when plural data having written into the memory at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.

18. A memory drive apparatus as claimed in claim 16, wherein the apparatus provides with addressing means for addressing the memory, and by sequentially addressing the

memory with the addressing means, plural data are arranged into the memory in matrix structures having n by n blocks, each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks.